Abstract of the Disclosure

An integrated circuit device for testing is disclosed. The device includes a plurality of internal circuits for generating a plurality of internal signals, the internal signals used for addressing storage locations and for controlling internal operations, a first selection circuit for receiving the internal circuits in response to selection signals corresponding to test information signals, a second selection circuit for receiving output signals from the first selection circuit and output signals from a sense amplifier, and for opening an alternative one of transfer paths of the internal signals and the output signals in response to the selection signals, and a data output buffer for transferring output signals from the second selection signals to an outside of the device through data input/output pads.